[0096] A video signal bus **35-1** through **35-16** carries analog video signals from digital to analog amplifiers (not shown) to column drivers **44***a-d*. Because signal interference and signal loss can occur as the analog video signal cross each signal line in the signal bus **35**, the channels of video signals are arranged to reduce interference. As illustrated, there are four column drivers **44***a*-**44***d*, two column drivers **44***a*,**44***b* at the top of the active matrix circuit **90** and two column drivers **44***c*,**44***d* at the bottom of the active matrix circuit region **90**. Each channel is allocated to one of the column drivers **44** such that each column driver **44** receives video from four channels. The top column drivers **44***a*,**44***b* receive video from the channels that drive the odd-numbered pixel columns and the bottom column drivers **44***c*,**44***d* receive video from the channels that drive the even-numbered columns. As shown, no video signal has to cross the path of more than one other video signal.

[0097] The illustrated arrangement of column drivers is particularly suited for edge-to-center and center-to-edge video writing, although the data can also be written from left-to-right or right-to-left. It should be understood that more or less than four column drivers **44** can be employed in preferred embodiments of the invention. For applications having resolutions of 320×240 or 640×480 it is desirable to use single column and row drivers to drive the display. For high speed, high definition displays more can be used to improve performance.

[0098] The data scanners **42***a-d* are responsive to a pixel data signal **142** and a pixel clock signal **143** from a control signal generator (not shown). The data scanners **42***a-d* can use a shift register array to store data for each scan. An odd shift register array can be used to store data to odd column pixels and an even shift register array can be used to store data to even column pixels. As illustrated, there are left and right odd data scanners **42***a*,**42***b* and left and right even data scanners **42***c*,**42***d*.

[0099] The column drivers **44** selected by the data scanner **42** transmit video data to a selected column of C pixels in the active matrix circuit **90**. The select scanner **46** controlled by a control signal generator determines by control lines which pixels accept this column data.

[0100] To reduce signal loss across the active matrix region **90**, the select lines are driven from both sides by select scanners **46***a* and b. As viewed in **FIG. 2A, a** left select scanner **46***a* and right select scanner **46***b* are connected to the select data line **146** and the select clock line **147**. A third enabling line **148** can also be used for specific applications. The left select scanner **46***a* provides a select line signal at the end of the select line nearest the lowest-valued pixel column (C_1) and right select scanner **46***b* provides a select line signal at the end of the select line nearest the highest-valued pixel column (C_N). Thus, an identical select line signal is supplied at both ends of the select line.

[0101] Although static shift registers can be used, the shift registers of the data scanner **42** and the select scanners **46** are preferably implemented as dynamic shift registers. The dynamic shift registers rely on capacitor storage without leakage. However, dynamic shift registers are susceptible to leakage, especially when they are exposed to light. Hence, light shields are needed to protect the scanners **42***a*-**42***d*,**46** from exposure to light. Similarly, light shields are also used to protect the transmission gates **44** and pixel columns C_1-C_N.

[0102] For further information regarding the input signals to the circuit **100**, reference is made to the above-cited U.S. patents and applications.

[0103] In a preferred embodiment of the invention, the panel drive circuitry of **FIG. 2A** is fabricated as an integrated circuit along with the active matrix circuit **90**. The integrated circuitry is preferably fabricated in single crystal silicon having a silicon-on-insulator (SOI) structure using the fabrication and transfer procedures described previously in the aforementioned U.S. Pat. No. 5,256,562. By fabricating the row and column drive circuitry **42***a*-**42***d*, **44***a*-**44***d*, **46***a*, **46***b* as well as the scanners in single crystal material along with the active matrix circuit **90**, the size of the display panel is not constrained by the connecting pins for the various discrete components. The integrated fabrication also increases the operating speed of the display relative to displays constructed from discrete components. Furthermore, the drive circuitry can be optimized to increase display performance. For example, it is easier to construct a small 1280H×1024V display panel with dual select scanners through integrated fabrication than it is using discrete components.

[0104] The pixel electrodes in a preferred embodiment are between 60 and 250 microns square. Consequently, a 1280H×1024V active matrix with the control system can be fabricated such that there are at least 40 such integrated circuits on a five inch wafer, for example.

[0105] A preferred embodiment of a display control circuit for a color sequential microdisplay is illustrated in connection with **FIG. 2B**. The display control circuit **102** receives an analog composite signal **103** such as a television or VCR video signal at converter **105**. Converter **105** can be a commercially available chip, such as the Sony CXA1585, which separates the signal **103** into red, green and blue components. The three analog color components are converted into digital signals by three respective analog to digital (A/D) converters **106**. The three color digital signals are stored in red **107**, green **108**, and blue **109** memory circuits. Circuits **107**, **108** and **109** can be RAM, such as DRAM, frame buffers that are connected to the timing circuit **110**. Timing circuit **110** can be connected to the converter **105** by an interface bus and receives horizontal and vertical synchronization signals along lines **119** from converter **105**. Circuit **110** controls the sequential flow of each color frame onto the display by sending video data from each memory **107**, **108**, **109** onto the display and coordinating actuation of the backlight **111** along lines **115** for each primary color. Lines **114** provide control of hue and contrast of the resulting image. Lines **116**, **117** and **118** are used to control the row and column driver circuits within display circuit **112**. Lines **116** and **117** control horizontal shift and vertical shift of the data as it is read onto the display.

[0106] Lines **116** and **117** can be used to allow the user to invert (i.e. reverse left to right or right to left) the image on the display. This can be useful for the telephone user who may select one hand to hold the telephone during use and simply press a button on the housing so that the image is inverted for presentation to the eye of the user when electing